

UNITED STATES PATENT APPLICATION

OF

SUNG JOON BAE

HAN SANG LEE

AND

JOON KYU PARK

FOR

DRIVING IC OF AN ACTIVE MATRIX ELECTROLUMINESCENCE DEVICE

**LONG ALDRIDGE & NORMAN LLP
701 PENNSYLVANIA AVENUE, N.W.
SUITE 600, SIXTH FLOOR
WASHINGTON, D.C. 20004
(202) 624-1200
(202) 624-1298**

[0001] This application claims the benefit of the Korean Application No. P2000-077083 filed on December 15, 2000, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a driving circuit of a display device, and more particularly, to a driving circuit of an active matrix electroluminescence device (AMELD) driven by digital signals.

Discussion of the Related Art

[0003] An AMELD emits light by electroluminescence. The AMELD is manufactured by forming electrodes of matrix type at both surfaces of a flat shaped luminescent layer. The AMELD includes a picture display unit and a driving circuit unit.

[0004] The AMELD has characteristics such as wide viewing angle, rapid response time, high contrast, low voltage driving, low power consumption, thinness and lightness in weight. Furthermore, the AMELD can display various colors, so that the AMELD has been attractive as a new generation display device for use in a large sized flat display device.

[0005] Display devices have several intermediate states, which range from black and white states to display various colors. At this time, methods for displaying colors are classified in two categories: (1) to adjust voltage intensity applied to a liquid crystal and (2) to adjust current intensity applied to the liquid crystal.

[0006] The method for adjusting the voltage intensity applied to the liquid crystal is based on a characteristic in which transmittivity of light varies according to the voltage

intensity. That is, picture luminance is changed according to a data voltage with respect to a threshold voltage by adjusting the intensity of an externally applied voltage.

[0007] At this time, the threshold voltage is the voltage at which a change of the transmittivity begins occur after a voltage is first applied, i.e. the threshold voltage is the gate voltage needed to establish a conducting channel between the source and drain of an enhancement MOS or PN Diode. If the threshold voltage is high, the voltage intensity applied to the liquid crystal must be increased, thereby increasing power consumption.

[0008] The transmittivity is proportional to the voltage intensity according to a curve function. In this case, it is hard to adjust the voltage intensity according to the transmittivity.

[0009] To obtain picture images in a display panel, several blocks are set to display gray so that transmittivity is changed according to the voltage intensity applied. At this time, if the blocks are set according to the voltage intensity, intervals of the transmittivity are not constant because the transmittivity is proportional to the voltage intensity in the curved function. Therefore, it is difficult to display gray and to obtain uniformity of the picture images.

[0010] Meanwhile, the transmittivity is proportional to the current intensity in a straight line. Therefore, to adjust the current intensity is easier and more accurate than to adjust the voltage intensity.

[0011] A driving circuit of a general AMELD will be described with reference to the accompanying drawings.

[0012] FIG. 1 is a schematic view showing a structure of the driving circuit of the general AMELD.

[0013] As shown in FIG. 1, the driving circuit of the general AMELD includes a power supply 10, an interface unit 11, a memory unit 12, a source driver 15, a gate driver 16 and a timing controller 17.

[0014] The power supply 10 supplies power to a display panel. The interface unit 11 transfers an image signal from an external micro controller. The memory unit 12 stores the image signal from the interface unit 11. The source driver 15 outputs the power supplied from the power supply 10 to a data signal of a display panel. Also, the gate driver 16 outputs a scan signal turning on a TFT to apply the data signal to each pixel of the display panel 18. The timing controller 17 generates and controls timing signals required to the source and gate drivers.

[0015] The signal source is a computer or a laser disk player for displaying moving pictures.

SUMMARY OF THE INVENTION

[0016] Accordingly, the present invention is directed to a driving circuit of an active matrix electroluminescence device (AMELD) that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0017] An advantage of the present invention is to provide a driving circuit of an AMELD that can control an output current value according to red, green and blue (R/G/B) channels by receiving a digital signal of n bits, thereby improving packing density of an integrated circuit (IC) for driving current.

[0018] Additional advantages and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0019] To achieve these advantages and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, in a driving circuit of an AMELD having data and gate drivers that respectively transmit a data signal and a scan signal to each pixel region, the data driver includes a latch latching a control signal temporarily stored, and a plurality of digital to analog converters (DAC) outputting a reference current of a certain level as a data signal according to R/G/B channels by the control signal latched.

[0020] That is, n number of reference current values temporarily set are selectively turned on according to digital signals of n bits for displaying gray desired. Also, two voltage terminals are formed, in which one has a constant voltage value, and the other has a voltage value that is changed according to R/G/B channels. Therefore, it is possible to adjust output voltage terminal according to R/G/B colors.

[0021] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0023] FIG. 1 illustrates a schematic view showing a structure of a driving circuit in a general AMELD;

[0024] FIG. 2 illustrates a structure view of a data driving circuit in a general AMELD;

[0025] FIG. 3 illustrates a circuit diagram of a driving circuit in an AMELD according to a first embodiment of the present invention;

[0026] FIG. 4 illustrates a circuit diagram of a driving circuit in an AMELD according to a second embodiment of the present invention;

5 [0027] FIG. 5 illustrates a circuit diagram of a driving circuit in an AMELD according to a third embodiment of the present invention;

[0028] FIG. 6 illustrates a circuit diagram of a driving circuit in an AMELD according to a fourth embodiment of the present invention;

10 [0029] FIG. 7 illustrates a circuit diagram of a driving circuit in an AMELD according to a fifth embodiment of the present invention;

[0030] FIG. 8 illustrates a circuit diagram of a driving circuit in an AMELD according to a sixth embodiment of the present invention;

[0031] FIG. 9 illustrates a circuit diagram of a driving circuit in an AMELD according to a seventh embodiment of the present invention;

15 [0032] FIG. 10 illustrates a circuit diagram of a driving circuit in an AMELD according to an eighth embodiment of the present invention;

[0033] FIG. 11 illustrates a circuit diagram of a driving circuit in an AMELD according to a ninth embodiment of the present invention;

20 [0034] FIG. 12 illustrates a circuit diagram of a driving circuit in an AMELD according to a tenth embodiment of the present invention;

[0035] FIG. 13 illustrates a circuit diagram of a driving circuit in an AMELD according to an eleventh embodiment of the present invention;

[0036] FIG. 14 illustrates a circuit diagram of a driving circuit in an AMELD according to a twelfth embodiment of the present invention;

[0037] FIG. 15 illustrates a circuit diagram of a driving circuit in an AMELD according to a thirteenth embodiment of the present invention;

[0038] FIG. 16 illustrates a circuit diagram of a driving circuit in an AMELD according to a fourteenth embodiment of the present invention; and

5 [0039] FIG. 17 illustrates a circuit diagram of a driving circuit in an AMELD according to a fifteenth embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

10 [0040] Reference will now be made in detail to the illustrated embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0041] A driving circuit in an AMELD according to the embodiments of the present invention will be described with the accompanying drawings.

15 [0042] FIG. 2 shows a structure of a data driver in a general AMELD.

[0043] As shown in FIG. 2, the data driver of the AMELD includes a shift register 24, a latch 26 and a digital-analog converter DAC 27.

20 [0044] Digital signals 20 of R/G/B (red/green/blue) channels input from external source according to a data clock 22 are temporarily stored in a shift register 24. Then, the latch 26 latches the digital signals 20 of the R/G/B channels applied from the shift register 24 according to control signals 28. The digital signals 20 of the R/G/B channels latched from the latch 26 are applied to the DAC. Then the DAC 27 converts the digital signals D_1 to D_n of the R/G/B channels to analog signals.

[0045] At this time, the DAC 27 includes a plurality of current DACs 27a, 27b, 27c.
25 In each current DAC 27a, 27b, 27c, the digital signals D_1 to D_n of the R/G/B channels are

temporarily combined by a plurality reference current sources I_1 to I_n that serve as control signals of a plurality of switching devices. Then a certain sink current is output to a data line connected to a pixel by outputting a current of a certain level.

First and Second Embodiments

[0046] FIG. 3 illustrates a circuit diagram of a driving circuit in an AMELD according to the first embodiment of the present invention. FIG. 4 illustrates a circuit diagram of a driving circuit in an AMELD according to the second embodiment of the present invention.

[0047] In the driving circuit of the AMELD according to the first embodiment of the present invention, the driving circuit includes a reference current output unit I and a sink current controller II.

[0048] In the reference current output unit I, a plurality reference current sources I_1 to I_n are temporarily combined, and then a reference current I_{ref} of a certain level is output. In the sink current controller II, a level of a sink current can be controlled by receiving the reference current I_{ref} of the certain level output from the reference current output unit.

[0049] The reference current output unit I includes a plurality of switching devices 30. Various currents I_1 to I_n of different levels are applied to input terminals of the switching devices 30. Output terminals of the switching device 30 are connected to one another. An output level in the output terminals 32, which are connected to one another, is determined by control signals D_1 to D_n .

[0050] In the present embodiment, the switching device is a TFT.

[0051] The sink current controller II includes a first voltage terminal V_1 , a second voltage terminal V_2 and a plurality of transistors T_n of current mirror type. A first transistor T_1 is connected between the first voltage terminal V_1 and the output terminal of the reference current output unit I. A second transistor T_2 is connected with the second voltage terminal

V_2 and a data line. Gates of the first and second transistors T_1 and T_2 are connected to the output terminal of the reference current output unit I.

[0052] In the digital driving circuit, the first voltage terminal V_1 is set at a constant value, such as a ground voltage. Alternatively, a positive voltage or a negative voltage can be used as a value of the first voltage terminal V_1 . Meanwhile, a certain voltage value is respectively applied to the second voltage terminal V_2 according to the R/G/B channels. In this case, if a voltage level is controlled, a level of the sink current can be increased or decreased, so that a certain voltage level is transmitted to the data line D/L.

[0053] At this time, levels of the reference current I_1 to I_n can be set temporarily like binary weight. That is, the level of the voltage is set so that an equation : $I_n = 2I_{n-1} = 2^2I_{n-2} = \dots = 2^{n-2}I_2 = 2^{n-1}I_1$ is satisfied. Or, the level of the reference voltage can be set in a gamma correction method.

[0054] The D_1 to D_n that serve as control signals are digital input signals of n bits, which are converted corresponding to input analog signals.

[0055] Meanwhile, as shown in FIG. 4, a driving circuit according to the second embodiment of the present invention includes further a current breaking switch S_1 between the output terminal of the reference current output unit I and the input terminal of the first transistor T_1 of the first embodiment of the present invention.

Third and Fourth Embodiments

[0056] FIG. 5 illustrates a circuit diagram of a driving circuit of an AMELD according to the third embodiment of the present invention. FIG. 6 illustrates a circuit diagram of a driving circuit of an AMELD according to the fourth embodiment of the present invention.

[0057] A driving circuit of the AMELD according to the third embodiment of the present invention includes a reference current output unit I and a sink current controller II.

[0058] The reference current output unit I includes a plurality of switching devices 50. Various currents I_1 to I_n of different levels are applied to input terminals of the switching devices, and output terminals of the currents are connected to one another. An output level in the output terminals 52, which are connected to one another, is determined by control signals D_1 to D_n .

[0059] In the present embodiment, the switching device is a TFT.

[0060] The sink current controller II includes a first voltage terminal V_1 , a first transistor T_1 , a fixed resistance R_s and a second transistor T_2 . The first transistor T_1 and the fixed resistance R_s are connected in series between the first voltage terminal V_1 and the output terminal 52 of the reference current output unit I. Also, the second transistor T_2 is connected in series between a data line D/L and the first voltage terminal V_1 . Gates of the first and second transistors are connected with the output terminal 52 of the reference current output unit I.

[0061] That is, the reference currents I_1 to I_n of different levels are applied and are selectively controlled and combined. Then, a reference current of a certain level is output from the reference current output unit I. The reference current of a certain level is input to gates of the first and second transistors T_1 , T_2 so that a voltage applied from the first voltage terminal V_1 can be controlled. Therefore, a value of a sink current I_{sink} from the data line D/L can be controlled. At this time, the voltage applied to the first voltage terminal is set any one of a ground voltage, a positive voltage and a negative voltage.

[0062] The resistance R_s is set so different levels according to the voltages of each of the R/G/B channels, thereby driving each R, G or B channel.

[0063] That is, even though the reference current I_{ref} is constantly outputted from the reference current output unit I, the value of the sink current I_{sink} according to each color can

be controlled by varying the fixed resistance R_s . Therefore, it is possible to obtain integration of the driving circuit in the AMELD.

[0064] In the present embodiment, the level of the reference current source is set temporarily. For examples, the voltage level V_1 is set so that an equation $I_n = 2I_{n-1} = 2^2I_{n-2} = \dots = 2^{n-2}I_2 = 2^{n-1}I_1$ is satisfied.

[0065] Meanwhile, as shown in FIG. 6, a driving circuit according to the fourth embodiment of the present invention includes further a current breaking switch S_1 between the output terminal 62 of the reference current output unit I and the input terminal 64 of the first transistor T_1 of the third embodiment of the present invention.

Fifth and Eighth Embodiments

[0066] FIG. 7 illustrates a circuit diagram of a driving circuit in an AMELD according to the fifth embodiment of the present invention.

[0067] As shown in FIG. 7, the driving circuit of the AMELD includes a reference current output unit I and a sink current controller II.

[0068] The reference current output unit I includes a plurality of switching devices 70. Various currents $I_1 \dots I_n$ of different levels are applied to input terminals of the switching devices 70. Then an output level in output terminals 72, which are connected to one another, is determined by control signals D_1 to D_n .

[0069] In the present embodiment, the switching device is a thin film transistor (TFT).

[0070] The sink current controller II includes a first voltage terminal V_1 , a variable resistance R_R , a first transistor T_1 , a fixed resistance R_s , a second transistor T_2 , and a third transistor T_3 . The transistors T_1 , T_2 and T_3 , are, for example, thin film transistors. At this time, the variable resistance R_R is connected in series between the first voltage terminal V_1 and the output terminal 72 of the reference current output unit I. The second transistor T_2 and

the third transistor T_3 are connected between a data line D/L and the first voltage terminal V_1 .
A gate of the third transistor T_3 is connected between the variable resistance R_R and a first
node N_1 connected to a drain of the first transistor. Gates of the first and second transistors T_1 ,
 T_2 are connected with a source of the second transistor T_2 and a second node N_2 connected to
5 a drain of the third transistor T_3 .

[0071] The variable resistance R_R value is adjusted to keep all of T_1 , T_2 , T_3 having an
equal characteristic in a panel when a data voltage is applied from the reference current
output unit.

10 [0072] The first and third transistors T_1 , T_3 include a current repeater, so that an
amount of current that flows from the data line to the first voltage terminal varies according
to an amount of current provided to the first node N_1 . That is, a reverse current that flows
through the second and third transistors T_2 , T_3 from the data line D/L to the first voltage
terminal V_1 varies according to the voltage of the reference current output unit I.

15 [0073] The first and second transistors T_1 , T_2 are formed in a current mirror, so that
an amount of current that is provided from the data line D/L to the first voltage terminal V_1 is
determined by an amount of current that flows in the third transistor T_3 .

[0074] A value of the fixed resistance R_s is determined according to R/G/B channels.
That is, in case that an equal pixel voltage is applied, the amount of current that flows from
the data line D/L to the first voltage terminal V_1 is determined according to a resistance value
20 of the fixed resistance R_s .

[0075] As shown in FIG. 10 illustrating the eighth embodiment, the fixed resistance
may be connected between the second transistor T_2 and the first voltage terminal V_1 .

[0076] The fixed resistance controls the voltage applied from the first voltage
terminal V_1 , thereby controlling a sink current I_{sink} value from the data line D/L. The voltage

applied to the first voltage terminal V_1 is set any one of a ground voltage, a positive voltage and a negative voltage.

[0077] That is, a reference current of a certain level output from the reference current output unit can control an output sink current value according to each R/G/B color. Therefore,
5 it is possible to obtain integration of the driving circuit in the AMELD.

[0078] Also, a luminance of a panel can be adjusted by controlling the variable resistance.

Sixth and Seventh Embodiments

[0079] FIG. 8 is a circuit diagram of a driving circuit in an AMELD according to the
10 sixth embodiment of the present invention. FIG. 9 is a circuit diagram of a driving circuit in an AMELD according to the seventh embodiment of the present invention.

[0080] As shown in FIG. 8, the driving circuit of the AMELD according to the present invention includes a reference current output unit I outputting a reference current I_{ref} of a certain level, and a sink current controller II controlling a level of a sink current I_{sink} .

[0081] The reference current output unit I includes n number of switching devices 80.
15 Various currents of different levels are applied to input terminals of the switching devices, and then reference currents $I_1 \dots I_n$ are combined by control signals D_1 to D_n of n bits, so that a certain output level is determined.

[0082] In the present embodiment, the switching device is a TFT.

20 [0083] The sink current controller II includes a first voltage terminal V_1 , a fixed resistance R_s , a first transistor T_1 and a second transistor T_2 . At this time, the first transistor T_1 is connected in series between the first voltage terminal V_1 and the output terminal of the reference current output unit I. The second transistor T_2 is connected with the fixed resistance R_s in series between a data line D/L and the first voltage terminal V_1 . Gates of the

first and second transistors T_1 and T_2 are connected with the output terminal 82 of the reference current output unit I.

[0084] The fixed resistance R_s is directly connected to the first voltage terminal V_1 . The first voltage terminal V_1 is set to be a constant voltage, and a sink current can be controlled according to each R/G/B channel by the fixed resistance R_s , which can be varied in value according to each R/G/B channel.

[0085] In the reference current output unit I, the n number of reference current sources are selectively combined by control signals D_1 to D_n of n bits, and then are output, thereby obtaining intermediate gray desired among R, G and B colors.

[0086] For example, if a driving circuit of 6 bits is used, 64 grays can be obtained. Also, if 256 grays are obtained in a full color monitor, at least sixteen million colors can be obtained.

[0087] As shown in FIG. 9, a driving circuit according to the seventh embodiment of the present invention includes further a current breaking switch S_1 between the output terminal 90 of the reference current output unit I and the input terminal N_1 of the first transistor T_1 of the sixth embodiment of the present invention.

Ninth, Tenth, Eleventh, Twelfth and Thirteenth Embodiments

[0088] FIG. 11 is a circuit diagram of a driving circuit of an AMELD according to the ninth embodiment of the present invention. FIG. 12 is a circuit diagram of a driving circuit of an AMELD according to the tenth embodiment of the present invention.

[0089] As shown in FIG. 11, the AMELD according to the ninth embodiment of the present invention includes a reference current output unit I and a sink current controller II. In the sink current controller II, a level of a sink current I_{sink} can be controlled by receiving the reference current output I_{ref} from the reference current output unit I.

[0090] At this time, the reference current output unit I includes a plurality of switching devices 110. Various currents $I_1 \dots I_n$ of different levels are applied to input terminals of the switching devices 110. Then an output level is determined in output terminals 112 connected to one another by control signals D_1 to D_n .

[0091] In the present embodiment, the switching device is a TFT.

[0092] The sink current controller II includes a first voltage terminal V_1 , and first, second, third and fourth transistors T_1 , T_2 , T_3 and T_4 .

[0093] The first and third transistors T_1 and T_3 are connected in series between the output terminal 112 of the reference current output unit I and the first voltage terminal V_1 . The second and fourth transistors T_2 and T_4 are connected in series between the first voltage terminal V_1 and a data line D/L.

[0094] At this time, gates of the third and fourth transistors T_3 , T_4 are connected to the output terminal 112 of the reference current output unit I, i.e., at a first node N_1 . Gates of the first and second transistors T_1 , T_2 are connected to an external bias voltage V_{Bias} which is controlled at a certain voltage.

[0095] The V_{Bias} is usually set at about 3.3V.

[0096] The voltage at the first voltage terminal V_1 is a voltage applied externally to control the level of the sink current I_{sink} output according to R/G/B channels.

[0097] Meanwhile, as shown in FIG. 12, a driving circuit according to the tenth embodiment of the present invention includes further a current breaking switch S_1 between the output terminal 122 of the reference current output unit I and the first node N_1 of the ninth embodiment.

[0098] As shown in FIG. 13, a driving circuit according to the eleventh embodiment of the present invention includes further a variable resistance R_R between the first node N_1 and the output terminal 132 of the reference current output unit I of the ninth embodiment.

The sink controller II, includes two voltage terminals: a first voltage terminal V_1 connected with a third transistor T_3 and a second voltage terminal V_2 connected with a fourth transistor T_4 . The first voltage terminal V_1 is set to be a constant value, such as a ground voltage. Alternatively, a positive voltage or a negative voltage can be used as a value of the first voltage terminal V_1 . Meanwhile, a certain voltage value is respectively applied to the second voltage terminal V_2 in accordance with the R/G/B channels. In this case, if the voltage level is controlled, a level of the sink current I_{sink} can be increased or decreased, so that a certain voltage level is transmitted to the data line D/L.

[0099] As shown in FIG. 14, a driving circuit according to the twelfth embodiment of the present invention includes further a variable resistance R_R between the output terminal 142 of the reference current output unit I and a first node N_1 , and a fixed resistance R_s between a third transistor T_3 and a first voltage terminal V_1 . A value of the fixed resistance R_s is determined according to R/G/B channels. That is, in case that an equal pixel voltage is applied, an amount of current that flows from the data line D/L to the first voltage terminal V_1 is determined according to the value of the fixed resistance. Accordingly, it is possible to control the sink current I_{sink} value according to each R/G/B color with an equal digital input signal.

[00100] In the twelfth embodiment of the present invention, a fixed resistance may be connected between a fourth transistor T_4 and a first voltage terminal V_1 shown in FIG. 15 of the thirteenth embodiment.

Fourteenth and Fifteenth Embodiments

[00101] FIG. 16 is a circuit diagram of a driving circuit of an AMELD according to the fourteenth embodiment of the present invention. FIG. 17 is a circuit diagram of a driving circuit of an AMELD according to the fifteenth embodiment of the present invention.

[00102] As shown in FIG. 16, the AMELD according to the fourteenth embodiment of the present invention includes a reference current output unit I and a sink current controller II. In the sink current controller II, a level of a sink current I_{sink} can be controlled by receiving the reference current I_{ref} output from the reference current output unit I.

5 [00103] At this time, the reference current output unit I includes a plurality of switching devices 160. Various currents $I_1 \dots I_n$ of different levels are applied to input terminals of the switching devices. Then an output level in output terminals 162, which are connected to one another, is determined by control signals D_1 to D_n .

[00104] In the present embodiment, the switching device is a TFT.

10 [00105] The sink current controller II includes a first voltage terminal V_1 , and first, second and third transistors T_1 , T_2 and T_3 .

15 [00106] At this time, the first transistor T_1 is directly connected to a data line D/L, and the second transistor T_2 is connected between the output terminal 162 of the reference current output unit I and the first voltage terminal V_1 . The first and third transistors T_1 and T_3 are connected in series between the data line D/L and the first voltage terminal V_1 .

[00107] Gates of the second and third transistors T_2 and T_3 are connected to a drain of the first transistor T_1 . A gate of the first transistor T_1 is connected to a first node N_1 between the output terminal 162 of the reference current output unit I and the input terminal of the first transistor T_1 .

20 [00108] In the above structure, a sink current I_{sink} value of each R/G/B channel can be controlled by applying a different voltage in accordance with the R/G/B channels to the first voltage terminal V_1 without varying the digital input signal, thereby improving packing density of an IC for driving current.

25 [00109] Meanwhile, as shown in FIG. 17, a driving circuit according to the fifteenth embodiment of the present invention includes further a current breaking switch S_1 between

the output terminal 172 of the reference current output unit I and a first node N_1 of the fourteenth embodiment.

[00110] As shown in FIG. 12, in a driving circuit according to the tenth embodiment of the present invention, a current breaking switch S_1 is additionally formed between the input terminal of the second transistor T_2 and the output terminal 172 of the reference current output unit I of the ninth embodiment of the present invention.

[00111] The current breaking switch S_1 of the second, fourth, seventh, tenth and fifteenth embodiments is formed to electrically disconnect the output terminal 172 of the reference current output unit I with the sink current controller II. Also, the current breaking switch S_1 is formed to decrease noise generated during turning on or off the switching devices by the D_1 to D_n that serve as control signals, so that it is possible to prevent undesired current consumption. (reference to FIGs. 4, 6, 9, 12 and 17)

[00112] In the present invention, the noise generated during turning on or off the switching device by the digital input signals of n bits is little, so that it is possible to form the driving circuit without regard for the noise as shown in the first, third, sixth, ninth and fourteenth embodiments of the present invention.

[00113] The driving circuit of the AMELD according to the present invention has the following advantages.

[00114] First, it is possible to drive the circuit according to each R/G/B channel with an equal digital input signal, thereby improving packing density of the IC for driving current.

[00115] Furthermore, the noise is little during turning on or off the digital input signal, so that it is not required to have the switching device for decreasing the noise.

[00116] It will be apparent to those skilled in the art than various modifications and variations can be made in the present invention. Thus, it is intended that the present invention

covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

400455434304